

JCS97 U.S. PTO  
09/904306

07/13/81

257	Class	666	Subclass	ISSUE CLASSIFICATION
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PATENT NUMBER

## U.S. UTILITY Patent Application

O.I.P.E. KS 563 SCANNED	PATENT DATE Q.A. JHT
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APPLICATION NO. 09/904306	CONT/PRIOR	CLASS 156 257	SUBCLASS 666+	ART UNIT 1733 2811	EXAMINER Q VU
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APPLICANTS  
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TITLE  
Interconnect circuitry, multichip module, and methods of manufacturing thereof

PTO-2040  
12/99

ISSUING CLASSIFICATION									
ORIGINAL				CROSS REFERENCE(S)					
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	666	257	667	668	773	774			
INTERNATIONAL CLASSIFICATION									
H01L	23/495								

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<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg. 13	Figs. Drwg. 39	Print Fig. 39	Total Claims 14	Print Claim for O.G. 1
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	_____ (Primary Examiner)			<b>ISSUE FEE</b>	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)			Amount Due	Date Paid
<b>ISSUE BATCH NUMBER</b>					
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